



Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS MEMORY DRIVERS

PRELIMINARY
IDT54/74FBT2240
IDT54/74FBT2240A

FEATURES:

- IDT54/74FBT2240 equivalent to the 54/74BCT2240
- **IDT54/74FBT2240A 25% faster than the 2240**
- 25Ω output resistors reduce overshoot and undershoot when driving MOS RAMs
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Higher static V_{OH} for improved noise immunity and reduced system power dissipation
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

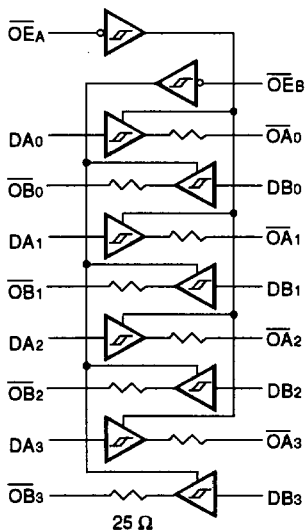
DESCRIPTION:

The FBT series of BiCMOS Memory Drivers is built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT2240 series are octal buffers/line drivers where each output is terminated with a 25Ω series resistor.

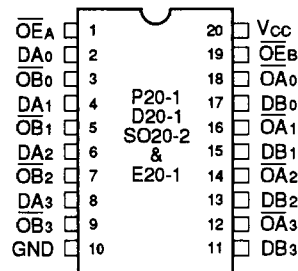
The FBT series of bus interface devices are ideal for use in designs needing to drive large capacitive loads with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection. The output buffers are designed to guarantee a static V_{OH} of 2.7V. This higher output level in the high state results in a significant reduction in overall system power dissipation and improved noise immunity when driving DRAMS and SRAMS.

FUNCTIONAL BLOCK DIAGRAM

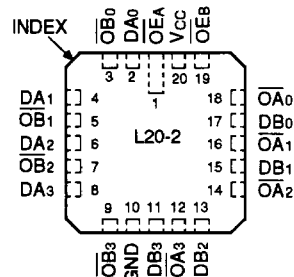


2642 drw 01

PIN CONFIGURATIONS



**DIP/SOIC/CERPACK
TOP VIEW**



**LCC
TOP VIEW**

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

APRIL 1992

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}A, \overline{OE}B$	3-State Output Enable Inputs (Active LOW)
Dxx	Inputs
$\overline{O}xx$	Outputs

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FUNCTION TABLE⁽¹⁾

Inputs		Output
$\overline{OE}A, \overline{OE}B$	Dxx	Oxx
L	L	H
L	H	L
H	X	Z

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	-0.5 to Vcc	-0.5 to Vcc	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	120	120	mA

NOTES:

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
- Input and Vcc terminals only.
- Outputs and I/O terminals only.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Type	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

NOTE:

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- This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: $V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Commercial: $T_A = 0^{\circ}C$ to $+70^{\circ}C$, $V_{CC} = 5.0V \pm 10\%$; Military: $T_A = -55^{\circ}C$ to $+125^{\circ}C$, $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$, $V_i = 2.7V$		—	—	10	μA
I_{IL}	Input LOW Current	$V_{CC} = \text{Max.}$, $V_i = 0.5V$		—	—	-10	μA
I_{OZH}	High Impedance	$V_{CC} = \text{Max.}$	$V_O = 2.7V$	—	—	50	μA
I_{OZL}	Output Current		$V_O = 0.5V$	—	—	-50	
I_I	Input HIGH Current	$V_{CC} = \text{Max.}$, $V_{CC} (\text{Max.})$		—	—	100	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}$, $I_N = -18mA$		—	-0.7	-1.2	V
I_{ODH}	Output Drive Current	$V_{CC} = \text{Min.}$, $V_O = 2.25V$		-35	—	—	mA
I_{ODL}	Output Drive Current	$V_{CC} = \text{Min.}$, $V_O = 2.25V$		50	—	—	mA
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}$, $V_O = GND^{(3)}$		-75	—	-225	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -300\mu A^{(4)}$	V_{HC}	V_{CC}	—	V
			$I_{OH} = -1mA$	2.7	3.8	—	
			$I_{OH} = -8mA$	2.4	3.3	—	
			$I_{OH} = -12mA$	2.0	3.2	—	
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 300\mu A^{(4)}$	—	GND	V_{LC}	V
			$I_{OL} = 1mA$	—	0.1	0.5	
			$I_{OL} = 12mA$	—	0.35	0.8	
			—	—	200	—	
I_{CCH}	Quiescent Power	$V_{CC} = \text{Max.}$		—	0.2	1.5	mA
I_{CCZ}	Supply Current	$V_{IN} = GND$ or V_{CC}		—	—	—	
I_{CCL}				—	—	—	

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NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0V$, $+25^{\circ}C$ ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This condition is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$, Outputs Open $\overline{OE}_A = \overline{OE}_B = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.3	0.40	mV/ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$, Outputs Open $f_i = 10\text{MHz}$, 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B = \text{GND}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.2	5.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	3.5	6.5	
		$V_{CC} = \text{Max.}$, Outputs Open $f_i = 2.5\text{MHz}$, 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B = \text{GND}$ Eight Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	6.2	9.5 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	8.2	17.5 ⁽⁵⁾	

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NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	IDT54/74FBT2240				IDT54/74FBT2240A				Unit
			Com'l.		Mil.		Com'L		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH	Propagation Delay	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	5.7	1.5	6.3	1.5	4.8	1.5	5.1	ns
tPHL	Dxx to Oxx										
tPZH	Output Enable Time		1.5	8.0	1.5	8.5	1.5	6.2	1.5	6.5	ns
tPHZ	Output Disable Time										
tPLZ			1.5	7.0	1.5	7.5	1.5	5.6	1.5	5.9	ns

NOTES:

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.

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